PCI Express® Architecture

Mobile Graphics Low-Power Addendum to the PCI Express® Base Specification Revision 1.0

October 21, 2003

Revision	Revision History	Date
1.0	Initial Release.	10/21/03

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Questions regarding this specification or membership in PCI-SIG may be forwarded to:

Membership Services
www.pcisig.com
E-mail: administration@pcisig.com
Phone: 503-619-0569
Fax: 503-644-6708

Technical Support
techsupp@pcisig.com

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Reference Documents

PCI Express Base Specification, Rev. 1.0a (PCI Express Base 1.0a)

PCI Express Card Electromechanical Specification, Rev. 1.0a (PCI Express CEM 1.0a)

PCI Express to PCI/PCI-X Bridge Specification, Rev. 1.0 (PCI Express Bridge 1.0)

Documentation Conventions

Capitalization

Some terms are capitalized to distinguish their definition in the context of this document from their common English meaning. Words not capitalized have their common English meaning. When terms such as "memory write" or "memory read" appear completely in lower case, they include all transactions of that type.

Register names and the names of fields and bits in registers and headers are presented with the first letter capitalized and the remainder in lower case.

Numbers and Number Bases

Hexadecimal numbers are written with a lower case "h" suffix, e.g., FFFh and 80h. Hexadecimal numbers larger than four digits are represented with a space dividing each group of four digits, as in 1E FFFF FFFFh. Binary numbers are written with a lower case "b" suffix, e.g., 1001b and 10b. Binary numbers larger than four digits are written with a space dividing each group of four digits, as in 1000 0101 0010b.

All other numbers are decimal.

Implementation Notes

Implementation Notes should not be considered to be part of this specification. They are included for clarification and illustration only.

Terms and Acronyms

Device	A logical device, corresponding to a PCI device configuration space. May be either a single or multi-function device.
Lane	A set of differential signal pairs, one pair for transmission and one pair for reception. A by-N Link is composed of N *Lanes*.
Link	The collection of two Ports and their interconnecting Lanes. A *Link* is a dual-simplex communications path between two components.
Port	1. Logically, an interface between a component and a PCI Express Link. 2. Physically, a group of Transmitters and Receivers located on the same chip that defines one end of a Link.
Receiver	The component that receives Packet information across a Link.
Transmitter	The component sending Packet information across a Link.

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1. Introduction

This addendum to the PCI Express Base 1.0a describes a low power extension intended primarily to support the reduced power requirements of mobile platforms. Its scope is restricted to the electrical layer and corresponds to Section 4.3 of PCI Express Base 1.0a.

1.1. Motivation

Mobile platforms are particularly sensitive to power requirements, while also not requiring the maximum interconnect loss defined in PCI Express Base 1.0a. For that reason, a low swing transmitter and a low loss interconnect is defined in this document to address the particular needs of mobile platforms. No changes are required in the receiver electrical specification.

In addition, any per Lane power savings is magnified due to the fact that mobile graphics utilizes up to a x16 PCI Express implementation.

1.2. Interoperability Requirements

In this document the following terms are used as defined below:

Standard Swing Transmitter. TX differential swing specified by $V_{TX\text{-}DIFFp\text{-}p\text{-}MIN}$ in Table 4-5 of PCI Express Base 1.0a.

Low Swing Transmitter. TX differential swing specified by $V_{TX\text{-}DIFFp\text{-}p\text{-}MIN}$ in Table 2-1 of this addendum.

Standard Loss Interconnect. An interconnect that allows a 13.2 dB maximum interconnect loss.

Low Loss Interconnect. An interconnect that allows a 7.2 dB maximum interconnect loss (see Section 2.2.5).

Interoperability requirements for a transmitting device, the system interconnect and receiving device are shown in Table 1-1. The transmitter and interconnect differ between PCI Express Base 1.0a and this addendum. As can be seen from Table 1-1, the only case that is not guaranteed to interoperate is when a low swing transmitter drives a standard loss interconnect.

Table 1-1: Interoperability Requirements

Transmitter/Channel	Low Loss Interconnect	Standard Loss Interconnect
Low Swing Transmitter	Yes	No
Standard Swing Transmitter	Yes	Yes

It is the responsibility of the system integrator to ensure interoperability.

Devices designed according to this addendum are not intended to be utilized with any of the standard electromechanical card form factors (PCI Express CEM 1.0a, ExpressCard 1.0, or any other electro-mechanical form factors unless otherwise specified).

In addition, any ability to configure a component to switch between a low swing Transmitter or a standard swing Transmitter is implementation specific and outside the scope of this document.

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2. PCI Express Base 1.0a Modifications

This addendum describes only those parameters that differ from PCI Express Base 1.0a. With the exception of those parameters explicitly defined in this addendum, all logical and electrical requirements in PCI Express Base 1.0a must be met.

2.1. Electrical Modifications Overview

The following is a summary of the electrical modifications required by this addendum:

- The minimum differential transmitter output voltage swing is reduced by 50%.
- Transmitter de-emphasis shall not be implemented.
- The maximum interconnect loss is reduced by 50%.

By limiting all required changes to the transmitter and interconnect, the receiver electrical specifications do not require modification.

IMPLEMENTATION NOTE

Power Savings

All power savings occur from implementing a reduced minimum differential transmitter output voltage swing. The two main sources of power savings are:

- Lower current and/or voltage needed by the output differential driver.
- Additional power savings may occur as a result of implementing a lower voltage supply for the entire PCI Express interface.

2.2. Electrical Details

A device that is compliant with this addendum must meet the following:

- With the exception of the electrical specifications defined below, a device must be compliant with PCI Express Base 1.0a.
- A device must be compliant with the electrical specifications defined in the following sections.

2.2.1. TX Output Differential Voltage

In Table 2-1, the minimum driver output voltage swing ($V_{TX\text{-}DIFFp\text{-}p\text{-}MIN}$) is reduced to 400 mV from 800 mV while maintaining a maximum swing of 1.2 V.

Table 2-1: Output Voltage Swing for Low Power Driver Specification

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak to Peak Output Voltage	**0.400**		1.2	V	$V_{TX\text{-}DIFFp\text{-}p} = 2*\|V_{TX\text{-}D+} - V_{TX\text{-}D-}\|$ See Note 1.

Notes:

1. Specified at the measurement point into a timing and voltage compliance test load as shown in Figure 2-1 and measured over any 250 consecutive TX UIs. (Also refer to the Transmitter compliance eye diagram shown in Figure 2-2.)
2. Voltage margins are measured over 250 consecutive Tx unit intervals. (Also refer to the Transmitter compliance eye diagram shown in Figure 2-2.)

2.2.2. TX Output De-emphasis

Due to the reduced loss budget, the need for transmitter de-emphasis is removed and must not be implemented. This means the amplitude of each bit, as measured into the test load shown in Table 2-2, is uniform no matter whether it is a transition bit or whether multiple bits of the same polarity are output in succession.

Table 2-2: De-emphasis for Low Power Driver Specification

Symbol	Parameter	Min	Nom	Max	Units	Comments
$V_{TX\text{-}DE\text{-}RATIO}$	De-emphasized Differential Output Voltage (Ratio)	**0.0**	**0.0**	**0.0**	dB	A low swing Transmitter must not use any de-emphasis.

2.2.3. Compliance Test and Measurement Load

The transmitter AC timing and voltage parameters must be verified at the measurement point, as specified by the device vendor, within 0.2 inches of the package pins, into the test/measurement load shown in Figure 2-1.

The allowance of the measurement point to be within 0.2 inches of the package pins is meant to acknowledge that package/board routing may benefit from D+ and D- not being exactly matched in length at the package pin boundary. If the vendor does not explicitly state where the measurement point is located, the measurement point is assumed to be the D+ and D- package pins.

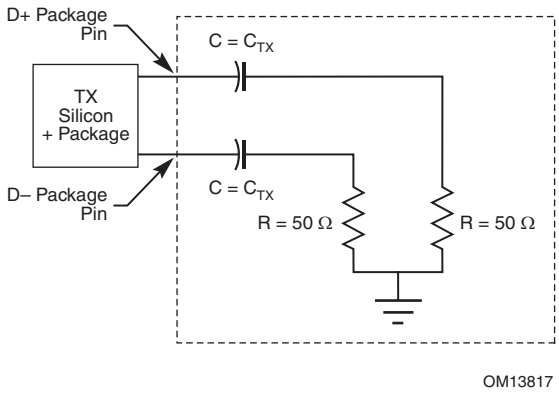

Figure 2-1: Compliance Test/Measurement Load

When measuring Transmitter output parameters, C_{TX} is an optional portion of the Test/Measurement load. When used, the value of C_{TX} must be in the range of 75 nF to 200 nF. C_{TX} must not be used when the Test/Measurement load is placed in the Receiver package reference plane.

2.2.4. Transmitter Compliance Eye Diagram

Compliance of the transmitter eye diagram uses the same methodology as outlined in PCI Express Base 1.0a. The Tx eye diagram is specified using the passive compliance/test measurement load (see Figure 2-1) in place of any real PCI Express interconnect plus Rx component. Because de-emphasis is not implemented, the transition and de-emphasized bit transitions are merged into a single Transmitter compliance eye diagram.

The eye diagram must be valid for any 250 consecutive UIs.

A recovered TX UI is calculated over 3500 consecutive unit intervals of sample data. The eye diagram is created using all edges of the 250 consecutive UI in the center of the 3500 UI used for calculating the TX UI.[1]

[1] It is recommended that the recovered TX UI be calculated using all edges in the 3500 consecutive UI interval with a fit algorithm using a minimization merit function (i.e., least squares and median deviation fits).

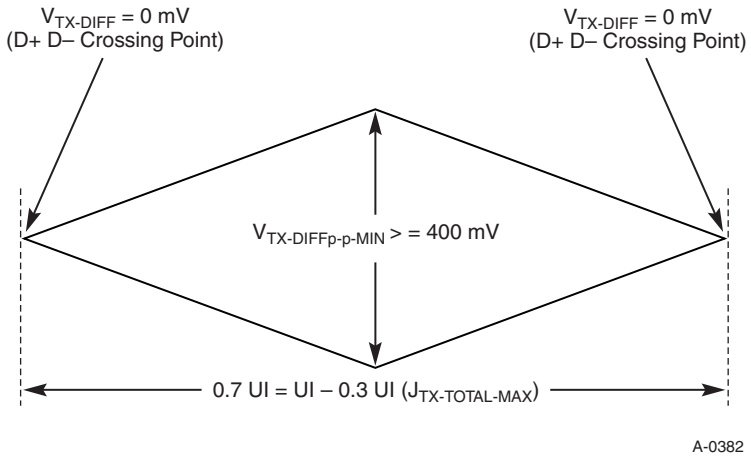

Figure 2-2: Transmitter Compliance Eye Diagram

2.2.5. Interconnect Loss

The modified worst-case interconnect loss budget is calculated by taking the minimum output voltage ($V_{TX-DIFF_{p-p}}$ = 400 mV) divided by the minimum input voltage to the Receiver ($V_{RX-DIFF_{p-p}}$ = 175 mV), which results in 7.2 dB.

2.3. Testing and Validation

All compliance and validation requirements for PCI Express Base 1.0a are applicable to this addendum with the exception of the Tx electrical modifications outlined above.

Acknowledgements

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Tan V Tran	Intel Corporation

[2] Company affiliation listed is at the time of specification contributions.